

Serial No. 09/177,814

IN THE CLAIMS:

Please amend the claims as follows:

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1. (Twice amended) A sample separation apparatus, comprising:

a [semiconductor] substrate including a material comprising at least one of silicon, gallium arsenide, and indium phosphide; and

a matrix formed of said material of said substrate, said matrix comprising a first porous region extending a distance across said [semiconductor] substrate.

B2 Subt
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4. (Twice amended) The sample separation apparatus of claim 1, wherein said first porous region linearly traverses said [semiconductor] substrate.

5. (Twice amended) The sample separation apparatus of claim 1, comprising a second porous region extending a distance across said [semiconductor] substrate.

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16. (Twice amended) The sample separation apparatus of claim 1, further comprising a processor on said [semiconductor] substrate.

17. (Twice amended) The sample separation apparatus of claim 1, further comprising a memory device on said [semiconductor] substrate.

B4 Subt
DC11
30. (Twice amended) A separation apparatus, comprising:
a substrate of a material;

at least one capillary column formed in said substrate of said material and comprising [a] first porous matrix; and

a detector situated adjacent said capillary column.

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51. (Twice amended) A miniature chromatograph, comprising:
a substrate of a material;

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~~a porous matrix formed in said substrate of said material and comprising at least one capillary column, said porous matrix comprising a plurality of pores.~~

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57. (Twice amended) An electrophoretic apparatus, comprising:
a [semiconductor] substrate including a material comprising at least one of silicon, gallium arsenide, and indium phosphide;
at least one sample column formed in said [semiconductor] material of said substrate and comprising a first end, a second end, and a first porous matrix which comprises a first plurality of pores; and
a control column comprising a second porous silicon matrix comprising a second plurality of pores formed in said [semiconductor] material of said substrate.

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64. (Twice amended) An analyte detection apparatus, comprising:
a [semiconductor] substrate comprising silicon; and
a matrix formed in said silicon of said [semiconductor] substrate, said matrix comprising at least one porous column.

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66. (Amended) The analyte detection apparatus of claim 64 [65], further comprising a capture substrate disposed on said matrix.

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72. (Twice amended) The analyte detection apparatus of claim 64, further comprising a control column on said [semiconductor] substrate.

REMARKS

The Final Office Action mailed January 3, 2000, has been received and reviewed. Claims 1, 3-64, 66-74, and 105-107 are currently pending in the application. Claims 1, 3-64, 66-74, and 105-107 stand rejected. Applicant proposes to amend claims 1, 4, 5, 16, 17, 30, 51,